Claims

What is claimed is:

1. A flip-flop controlled switcher comprising:

at least one flip-flop having a data input, a data output, and a control input; and

at least one transistor switch having a gate connected to said data output of said flip-flop wherein a state of said switcher is established by a state of said flip-flop.

2. A flip-flop controlled switcher of claim 1, wherein the gates of a plurality of transistor switches being connected to the data outputs of a plurality of flip-flops arranged as a shift register.

3. A flip-flop controlled switcher of claim 1, wherein said data output of said flip-flop further connects to a default value generating means that provides a default signal to the gate of said transistor switch.

4. A flip-flop controlled switcher of claim 3, wherein said default signal generating means comprising a first default signal line and a second default signal line, said second default signal line carries a complementary signal to said first default signal line, said first and second default signal lines being connected selectively to said data outputs of said flip-flops through a buffering means.

5. A flip-flop controlled switcher of claim 4, wherein said buffering means being a MOS transistor.

6. A flip-flop controlled switcher comprising:

A shift register having a plurality of serially-connected flip flops, each flip-flop having a data input, a data output, and a controlling input; and

a set of transistor switches each having a gate connected to said data output of each said flip-flop, wherein a state in each said switch is established by a state in said flip-flop connected to said gate of said switch.

7. A flip-flop controlled switcher in claim 6, wherein each flip-flop having a default state defined by a default generating means.

8. A flip-flop controlled switcher in claim 7, wherein said default generating means comprising a first default signal line and a second default signal line, said second default signal line carries a complementary signal to said first default signal line, said first and second default signal lines being connected selectively to said data outputs of said flip-flops through a buffering means.

9. A flip-flop controlled switcher of claim 8, wherein said buffering means being a MOS transistor.

10. A circuit for fine-tuning a voltage output comprising:

a set of resistors connected in parallel to the voltage output, each resistor being connected to ground through a switching transistor; and

a set of flip-flops connected to the gates of said switching transistors wherein a state in each said switching transistor being established by a state in a corresponding flip-flop, where one or more resistors may be connected to ground as determined by the states in said flip-flops.

11. A circuit of claim 10, wherein said data output of said flip-flop further connects to a default value generating means that provides a default signal to the gate of said transistor switch.

12. A flip-flop controlled switcher of claim 11, wherein said default signal generating means comprising a first default signal line and a second default signal line, said second default signal line carries a complementary signal to said first default signal line, said first and second default signal lines being connected selectively to said data outputs of said flip-flops through a buffering means.

13. A flip-flop controlled switcher of claim 12, wherein said buffering means being a MOS transistor.

14. A flip-flop controlled switches of claim 10, wherein the gates of a plurality of transistor switches being connected to the data outputs of a plurality of flip-flops arranged as a shift register.

15. A switch controlling circuit comprising N number of flip-flops, each of which having an input terminal and an output terminal, where N is any number greater than 1, said flip-flops being connected in a serial manner to form a chain with the input of a first flip-flop serving as an input to said flip-flop chain and the output of the last flip-flop serving as an output for said flip-flop chain, wherein said input of said flip-flop chain connects to an output of a multiplexer having a control terminal, a first input terminal and a second input terminal, said first input terminal of said multiplexer being connected a data input terminal while said second input terminal being connected to said output of said flip-flop chain, wherein said flip-flops are being programmed by shifting data in through said first input terminal of said multiplexer, wherein said outputs of said flip-flops being connected to controlling terminals of a plurality of switches, whereby signals at said outputs of said flip-flops activates or deactivates said switches.

16. A switch controlling circuit of claim 15, wherein the output of each said flip-flop further connects to drains of an NMOS transistor and a PMOS transistor, forming a common node that also serves as the output of the transistor pair, the source of said PMOS transistor being connected to a power supply while the source of said NMOS transistor being connected to a ground, the

gate of said NMOS transistor being connected either to a ground or a first default line while the gate of said PMOS transistor being connected either to a power supply or a second default line, said first default line, which carries a default signal of logic "1" connects to said second default line through an inverter, wherein said gates of said PMOS and NMOS transistor pair being connected to said second default line and said ground respectively for a desired default output logic value of "1", and wherein said gates of said PMOS and NMOS transistor pair being connected said power supply and said first default line for a desired default output logic value of "0".